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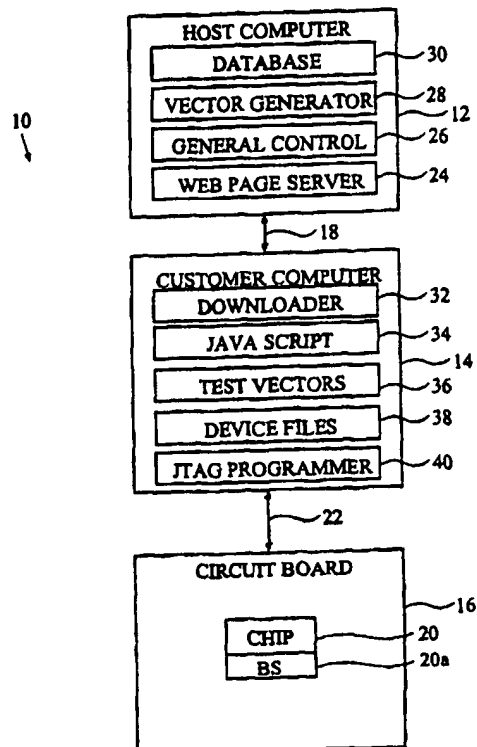
INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁷ : G06F 11/273		(11) International Publication Number: WO 00/48075
A1		(43) International Publication Date: 17 August 2000 (17.08.00)
(21) International Application Number: PCT/US00/01326 (22) International Filing Date: 19 January 2000 (19.01.00) (30) Priority Data: 09/249,907 12 February 1999 (12.02.99) US (71) Applicant: XILINX, INC. [US/US]; 2100 Logic Drive, San Jose, CA 95124 (US). (72) Inventors: JENKINS, Jesse, H., IV; 72 Blackhills Place, Danville, CA 94506 (US). EDMONDSON, Walter, H.; 405 Bryce Drive, Morgan Hill, CA 95037 (US). (74) Agents: YOUNG, Edel, M. et al.; Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124 (US).		(81) Designated States: JP, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published With international search report.

(54) Title: METHOD FOR REMOTELY TESTING MICROELECTRONIC DEVICE OVER THE INTERNET

(57) Abstract

The Internet is used to test an integrated circuit chip that is provided with boundary scan circuitry and plugged into a circuit board at a customer's location. A host computer at the manufacturer's location runs a web page server having the ability to remotely test a customer's chip. The process is initiated by the customer connecting the circuit board to his own computer and logging onto the web site. The customer transmits customer identification and other data to the web server, which then transmits a downloader program and a JAVA program script to the customer's computer. The customer's computer then uses the downloader program to transmit high and low level device data describing the functionality of the chip to the host computer, which then generates and transmits a set of suitable test vectors to the customer's computer. Then, the customer's computer tests the chip using the boundary scan circuitry and test vectors and transmits the test results to the host computer, which then produces and transmits an evaluation of the results to the customer's computer.



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1 METHOD FOR REMOTELY TESTING MICROELECTRONIC DEVICE
OVER THE INTERNET

FIELD OF THE INVENTION

6 The present invention generally relates to the art of
microelectronic integrated circuits, and more specifically
to a method for remotely testing an integrated circuit chip
or other microelectronic device over the Internet.

11

BACKGROUND OF THE INVENTION

Very large integrated circuit chips such as Programmable Logic Devices (PLD) and Application Specific Integrated Circuits (ASIC) are extremely intricate devices that are fabricated using a large number of precise and critical processing steps. Unfortunately, technology has not advanced to the point at which such a device can be fabricated with perfect reliability and be expected to never fail.

There are many ways in which a device can partially or completely malfunction, and it can be difficult to diagnose the source of a particular failure mode. The problem is exacerbated by the fact that integrated circuits are not used by themselves, but are components that are plugged into sockets on circuit boards that also include a number of other interconnected components. A particular malfunction can be the result of not only an internal fault in a chip, but from other components on the board and/or the manner and functionality in which the components are interconnected.

31 Programmable integrated circuit devices such as PLDs are fabricated and subjected to extensive testing at a manufacturing facility, and then shipped to customers who program the devices to implement their own required functionality. The programmed devices are assembled onto boards as described above and connected to power supplies and additional components to produce finished electronic products. The boards often include nonvolatile memories that

1 program the PLDs ever time power is turned on. These
products are then tested and shipped to consumers.

 A PLD or other device can fail immediately or after a
period of use. The testing procedure for a finished product
occurs both at the time of its initial manufacture and when
6 it is returned to the manufacturer for repair.

 In order to facilitate testing of large integrated
circuits such as PLDs, a methodology has been formulated by
the Joint Test Action Group (JTAG) and codified as IEEE
specification no. 1149.1. The methodology includes adding
11 special microelectronic components known as "boundary scan
circuitry" to the integrated circuit chips. This circuitry
enables test signals known as "vectors" to be applied to the
input pins of the chip and resulting output signals to be
read at the output pins. Although the testing can be
16 performed without removing a chip from its socket, the
testing is isolated to the internal functionality of the chip
and is unaffected by the other components on the board.

 Depending on the manner in which the individual elements
of the chip are fabricated or programmed to perform a
21 particular function, a set of test vectors is generated such
that every testable logic element in the chip will be
subjected to a test that determines if the individual element
is functioning properly. For every input vector there will
be a resulting output signal that will have a particular
26 value if there is no malfunction. If the actual output
signals match the expected values, the testing will indicate
that there are no damaged or malfunctioning elements in the
chip.

 Although boundary scan circuitry is provided in a large
31 number of integrated circuit chips being currently
fabricated, many customers do not have the ability to perform
the tests and/or generate a suitable set of test vectors.
If there is a malfunction, they return the chip to the
manufacturer with an indication that it did not function
36 properly. Often a customer will ask the manufacturer to test
the chip and/or troubleshoot the problem.

1 Manufacturers generally have a procedure known as
"return material authorization (RMA)" by which the customer
calls the manufacturer to obtain an RMA number and returns
the chip by mail with the RMA number marked on the outside
of the package. Preferably, the customer will inform the
6 manufacturer either at the time of the call or by means of
a letter in the package as to the nature of the problem.

 When the manufacturer receives the allegedly defective
chip, the chip will be sent to a failure analysis (FA) group
which performs a series of tests on the chip to determine if
11 it is in fact defective. If the customer provided device
data in the form of device specific program code indicating
the functionality that was programmed into the chip, the FA
group can generate a set of test vectors specific to the chip
and perform boundary scan testing. The FA group can make
16 internal tests as well. This testing can also be performed
using a generic set of test vectors.

 Other tests include physical examination of the chip,
typically using a microscope, to locate damaged pins, etc.
The protective cap can also be removed and the semiconductor
21 die itself can be examined under a microscope.

 Assuming that the chip itself is defective, the FA group
will hopefully isolate the cause of the defect and thereby
produce a solution to the problem. However, it is often the
case that the chip is not defective, but is programmed
26 improperly and/or integrated with the other components on the
circuit board to cause logical, signal or timing errors. A
solution to a problem of this type cannot be found by testing
the chip itself.

 The RMA/FA procedure as presently being practiced is
31 subject to several serious drawbacks. First, the chip must
be physically removed from the apparatus in which it is
incorporated and shipped to the manufacturer. This takes an
undesirably long time during which the apparatus is
unavailable and inaccessible for further troubleshooting.
36 In addition, removal of the chip can result in damage to the
pins.

1 The FA procedure is also lengthy and labor intensive.
This means that the customer must wait an extended period of
time for a solution to his problem, which is especially
undesirable either if the apparatus is in the process of
development or if the board is left inoperable.

6 Further, the FA analysis may not produce an answer to
the problem if the error was in another component that was
connected to the chip. For these reasons, a need exists in
the art for a method of quickly testing a customer's
integrated circuit chip in his own facility and in the
11 environment in which it is functionally connected.

SUMMARY OF THE INVENTION

16 The present invention overcomes the drawbacks of the
prior art and provides a method that enables an integrated
circuit chip to be quickly tested remotely and in situ.

21 More specifically, the present invention uses the
Internet or other electronic communication media to test an
integrated circuit chip that is provided with boundary scan
or other suitable circuitry and plugged into a circuit board
at a customer's facility.

26 A host computer at the manufacturer's facility runs a
web page server including the ability to remotely test a
customer's chip. The process is initiated by the customer
connecting the circuit board to his own computer and logging
onto the web site. The customer transmits identification and
other data to the web server, which then transmits a
downloader program and a JAVA program script to the
customer's computer. Alternatively, the downloader program
31 can be previously supplied to the customer and used to log
onto the web site.

36 The customer's computer then uses the downloader program
to transmit high and low level device data describing the
functionality of the chip to the host computer, which then
generates and transmits a set of suitable test vectors to the
customer's computer. Then, the customer's computer tests the

1 chip using the boundary scan circuitry and test vectors and
transmits the test results to the host computer, which then
produces and transmits an evaluation of the results to the
customer's computer.

6 These and other features and advantages of the present
invention will be apparent to those skilled in the art from
the following detailed description, taken together with the
accompanying drawings, in which like reference numerals refer
to like parts.

11

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating the components
used in practicing a method according to the present
invention for remotely testing an integrated circuit chip or
16 other device using the Internet;

FIG. 2 is a flowchart illustrating the present method;

FIG. 3 is a flowchart illustrating the method steps
performed by a host computer illustrated in FIG. 1; and

FIG. 4 is similar to FIG. 3, but illustrates the steps
21 performed by a customer's computer.

DETAILED DESCRIPTION OF THE DRAWINGS

Referring to FIG. 1 of the drawing, a system 10 for
26 remotely testing an integrated circuit chip or other
microelectronic device generally includes a host computer 12,
a customer's computer 14 and a circuit board 16. The host
computer 12 is provided at a manufacturer's location, whereas
the customer's computer is provided at a customer's location
31 that is remote from the manufacturer's location. Computers
12 and 14 are typically personal or workstation general
purpose computers and are interconnected by the Internet or
other electronic communication such as a Wide Area Network
(WAN) or Local Area Network (LAN) as symbolically indicated
36 at 18.

A Programmable Logic Device (PLD) or other integrated

1 circuit chip 20 that is to be tested remotely is plugged into
a socket (not shown) or otherwise operatively connected to
circuit board 16, which includes other components (not shown)
that functionally interact with chip 20. Circuit board 16
is connected to the customer's computer 14 using a cable of
6 the type that is conventionally used for Joint Test Action
Group (JTAG) boundary scan testing and is symbolically
indicated at 22. Chip 20 is provided with JTAG boundary scan
circuitry 20a which is conventionally implemented in
accordance with IEEE specification 1149.1.

11 Computers 12 and 14 include elements such as a
microprocessor, memory, etc. that are conventional and will
not be described in detail. Host computer 12 is programmed
with a number of software program and data code modules
including an Internet World Wide Web (WWW) server 24, a
16 general control program 26, a vector generator 28 and a
device and vector database 30.

The customer's computer 14 is programmed with a
downloader program 32, a JAVA script 34, test vectors 36,
design files 38 and a JTAG programmer 40.

21 Although the preferred embodiment of the invention that
will be described below utilizes JAVA script to perform the
required control functions, the invention is not so limited.
For example, ActiveX controls or any other suitable
programming language can be employed to implement this
26 functionality.

An overall flowchart of the present method is
illustrated in FIG. 2. As indicated by a step 50, the
customer or client initiates the process by using the
customer's computer 14 and the Internet 18 to log onto the
31 web site implemented by web page server 24 in host computer
12. After logging on, the customer's computer 14 will
preferably provide client identification data to host
computer 12 either automatically, or by the customer manually
filling out a form including entries for the customer
36 (client) name, company, identification number, version of the
software used to create the design (program the chip 20), and

1 e-mail address.

The JTAG programmer 40 and the downloader program 32 are preferably provided free of charge to the customer on a floppy disk or the like. Alternatively, either or both of programs 32 and 40 can be downloaded to the customer's computer 14 from host computer 12 after logging onto web site 24.

The program code for logging onto the web site can be implemented in downloader program 32 if it is initially provided to the customer. Alternatively, the customer's computer 14 can log onto the web site at the host computer 12 using a conventional Internet browser program such as Netscape® or Microsoft Internet Explorer® and download the downloader program 32 from the web site.

Assuming that chip 20 is a PLD or other programmable element that is programmed by the customer, design files 38 will be specific to chip 20 and will include several types of high and low level files. A high level design file will be a design source code file written in HDL Verilog® or other language that represents the desired logic function of chip 20. A high level design file can also be a design created by schematic capture. A low level design file will be a bitstream file that is essentially a compiled version of the high level design file. Design files 38 will preferably also include a Boundary Scan Description Language (BSDL) file that specifies the interconnections of boundary scan circuitry 20a.

In a next step 52, the customer's computer 14 may transmit the high and low level design files to host computer 12. The first test procedure is to compare the high and low level design files to determine if the low level file is properly derived (compiled) from the high level file. This can be performed either by the host computer 12 or by the JAVA script file 34 at the customer's computer 14.

In either case, the computer 12 or 14 that performed the test will preferably transmit a notification to the other computer as to the result of the test, or at least an

1 indication of whether the test failed. At this point, a
message can be displayed on either or both of computers 12
and 14 and the test procedure suspended. The test should be
suspended because a lack of correspondence between the high
and low level design files can be at least one source of the
6 problem, and no further testing may be appropriate until this
discrepancy is evaluated. The file evaluation can be
performed by personnel at either the manufacturer's or the
customer's location.

Assuming that these files correspond to each other, upon
11 receipt of the high and low level design files, in step 54,
vector generator 28, under control of general control unit
26, accesses vector database 30 and generates a set of test
vectors for testing chip 20, and in step 56 transmits the
vectors to the customer's computer 14. These are the test
16 vectors designated as 36 in FIG. 1.

The preferred embodiment of the invention that will be
described below utilizes test vectors in the form of digital
bit streams that are intended for boundary scan testing under
IEEE specification no. 1149.1. However, the scope of the
21 invention is not limited to digital testing, and the term
"test vectors" in the context of the invention will also be
considered to include test data for analog parametric
testing, and any other digital or analog testing that can
be implemented using a method of the invention.

26 Assuming that the design files 38 were either
transmitted from the customer's computer in step 52, or were
alternatively available at the host computer 12, vector
generator 28 will access database 30 and generate a set of
test vectors that is specific to the design or functionality
31 programmed into chip 20.

As an alternative, if the design files were not
available to the host computer for security or other reasons,
or chip 20 was not programmed, vector generator 28 will
access database 30 and provide a set of generic test vectors
36 that are suitable to the model number of chip 20 as supplied
by the customer's computer 14.

1 As yet another alternative within the scope of the invention, specific or generic test vectors can be generated in advance either by the manufacturer or by the customer and stored as part of design files 38 in the customer's computer 14.

6 In the next step, designated as 58, the customer's computer 14 tests the device (chip 20) using boundary scan circuitry 20a and test vectors 36 to produce test results. This is performed by JTAG programmer program 40 under control of JAVA script 34, as will be described below. Then, in step 11 60, the customer's computer 14 transmits the test results to host computer 12. In step 62, host computer 12 evaluates the test results to determine if the boundary scan testing produced an indication of a malfunction.

16 The result is a failure evaluation, which in step 64 host computer 12 transmits to the customer's computer 14 and the customer's computer 14 displays on a monitor and/or prints out as a report to the customer. As an alternative, JAVA script 34 or other software provided at the customer's computer 14 can perform the evaluation and transmit an 21 evaluation to host computer 12.

FIG. 3 illustrates the individual method or process steps that are performed by the customer's computer 14. First, in step 70, downloader program 32 or a web browser is used to locate and input the client identification and design 26 files 38. Preferably, design files 38 will be stored in a single predetermined subdirectory and can be automatically located. The client identification data can be stored in a text file in the same subdirectory as design files 38. Alternatively, the client identification data can be manually 31 input by the customer after logging onto the web site.

In step 72, the customer's computer 14 logs onto the host computer's web page server 24, and in step 74 uploads the client identification data and device data. In step 76, the customer's computer 14 then downloads or receives JAVA 36 script 34 and test vectors 36 from host computer 12. In step 78, JAVA script 34 is launched and controls JTAG programmer

1 40 to perform the boundary scan testing as described above,
and produce test results that in step 80 are uploaded to host
computer 12. In step 82, the customer's computer 14 then
downloads and displays the evaluation of the test results
from host computer 12.

6 The JAVA script 34 enables the entire testing and
evaluation process to be performed automatically under
control of host computer 12 after receiving the request and
data from the customer's computer 14. However, alternatives
to the JAVA implementation are possible within the scope of
11 the invention. For example, the functionality of JAVA script
34 can be pre-stored as a separate program on the customer's
computer 14 or implemented by downloader program 32, and
launched by a script or other command from host computer 12.

16 The method steps performed by host computer 12 are
illustrated in FIG. 4. In step 90, after the customer's
computer 14 logs onto web page server 24, host computer 12
downloads client identification and device data as described
above. Then in step 92, host computer 12 compares the high
and low level design data and transmits an evaluation of this
21 test to the customer's computer 14 if appropriate. Then in
step 94, vector generator 28 generates test vectors 36, and
in step 96 uploads vectors 36 to the customer's computer 14.

After completion of the boundary scan testing by host
computer 12, in step 98 the customer's computer 14 downloads
26 the test results, in step 100 processes the results to
generate an evaluation, and in step 102 uploads the
evaluation to the customer's computer 14.

In view of the above detailed description, it will be
seen how the present invention is highly advantageous over
31 the prior art. A customer can test a chip in situ and be
automatically provided with results in minutes or less as
compared to days or more in the prior art. No special
operations or knowledge are required of the customer. All
he has to do is connect board 16 to the customer's computer
36 14 using cable 22, call up and log onto the web site at host
computer 12, and let the system 10 do the rest with minimal

1 downtime of the customer's equipment.

 The chip 20 does not have to be removed from board 16
and be subjected to potentially damaged pins, etc. The
present method performs the boundary scan testing in situ and
thereby determines definitively if the problem is chip 20
6 itself, external to chip 20 or due to an interconnection
problem with other components on board 16. The level of
speed and customer service provided by the present invention
have been lacking and long desired in the art.

 Various modifications will become possible for those
11 skilled in the art after receiving the teachings of the
present disclosure without departing from the scope thereof.
For example, one or more of the method steps can be performed
semi-manually or manually, such as the customer and
manufacturer transmitting information and files to each using
16 e-mail and attachments. In this case, each party will wait
for the appropriate response from the other before performing
their next step.

 It is also within the scope of the invention to perform
all of the testing and analysis using the customer's
21 computer. In this case, all necessary software modules would
be provided to the client either on media such as CD ROMs or
floppy disks, or downloaded from the host computer. The
customer would then run the software on his computer and
evaluate the problem based on results of the testing.

1

CLAIMS**WHAT IS CLAIMED IS:**

1. A method for testing an electronic device connected to a customer's computer, comprising the steps of:

6 a) controlling the customer's computer to transmit test request data to a host computer;

b) controlling the host computer to transmit test vectors to the customer's computer;

11 c) controlling the customer's computer to test the device using the test vectors and generate test results; and

d) processing the test results to generate an evaluation.

16 2. A method as in claim 1 in which the steps are performed in the order indicated.

21 3. A method as in claim 1, in which step (d) is performed by the customer's computer.

4. A method as in claim 1, in which step (d) is performed by the host computer; and

26 the method further comprises the step, performed between steps (c) and (d), of:

(e) controlling the customer's computer to transmit the test results to the host computer.

31

5. A method as in claim 3, in which the method further comprises the step of:

(f) controlling the host computer to transmit the evaluation to the customer's computer.

36

1 6. A method as in claim 1, in which:
 the test request data includes device specific data;
and
 the method further comprises the step, performed
between steps (a) and (b), of:
6 (e) generating the test vectors in accordance with the
device specific data.

11 7. A method as in claim 1, in which the test vectors are
generic test vectors.

16 8. A method as in claim 1, in which:
 the device comprises boundary scan circuitry;
 the test vectors are boundary scan test vectors; and
 step (c) comprises testing the device using boundary
scan test software.

21 9. A method as in claim 1, in which:
 the test request data comprises high level device data,
and low level device data that is derived from the high level
device data; and
 the method further comprises the steps of:
26 (e) determining if the low level device data is
properly derived from the high level device data; and
 (f) generating an indication of whether or not the low
level device data is properly derived from the high level
device data.

31

10. A method as in claim 8, in which steps (e) and
(f) are performed by the host computer.

36

11. A method as in claim 8, in which steps (e) and

1 (f) are performed by the customer's computer.

12. A method as in claim 1, in which:

6 step (b) further comprises controlling the host computer to transmit test program code to the customer's computer, which causes the device to be tested using the test vectors and generate the test results; and

step (c) comprises controlling the customer's computer to run the test program code.

11

13. A method as in claim 11, in which the test program code comprises a script file.

16

14. A method as in claim 11, in which the test program code comprises JAVA script.

21 15. A method as in claim 1, in which:

the host computer comprises a web page server; and

the method further comprises the step, performed prior to step (a), of:

26 (e) controlling the customer's computer to log onto the web page server.

16. A method as in claim 14, in which:

31 step (b) comprises controlling the web page server to transmit the test vectors to the customer's computer;

step (b) further comprises controlling the web page server to transmit test program code to the customer's computer, which causes the device to be tested using the test vectors and generate the test results; and

36 step (c) comprises controlling the customer's computer to run the test program code.

1

17. A method as in claim 15, in which the test program code comprises a script file.

6

18. A method as in claim 14, in which:
the web page server stores a downloader program that causes the customer's computer to perform steps (b) and (d);
and

11

the method further comprises the step, performed
between steps (e) and (a), of:
(f) controlling the customer's computer to download the downloader program from the host computer and run the downloader program.

16

19. A method as in claim 17, in which the downloader program further causes the customer's computer to perform step (a).

21

20. A method as in claim 17, in which step (e) comprises controlling the customer's computer to transmit client identification data to the web page server.

26

21. A method as in claim 19, in which:
the test request data includes device data; and
the downloader program causes the device data to be uploaded to the web page server in step (a).

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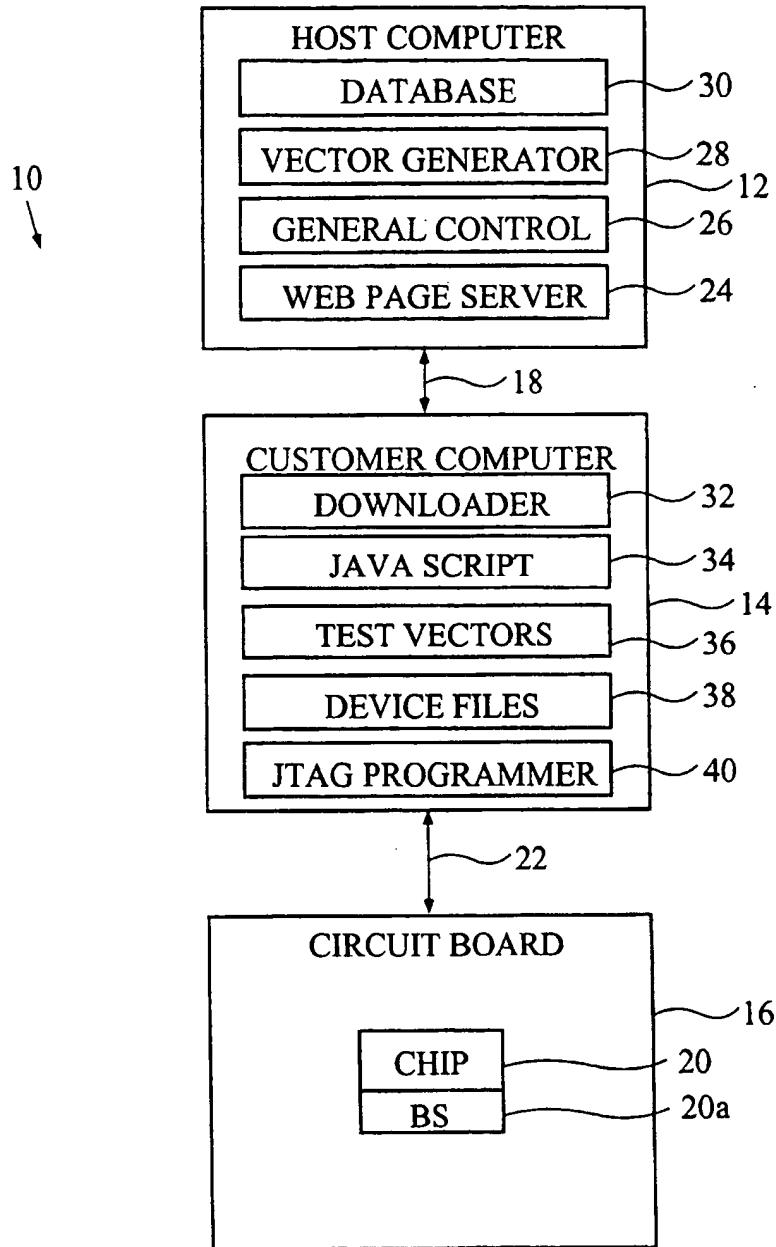


FIG. 1

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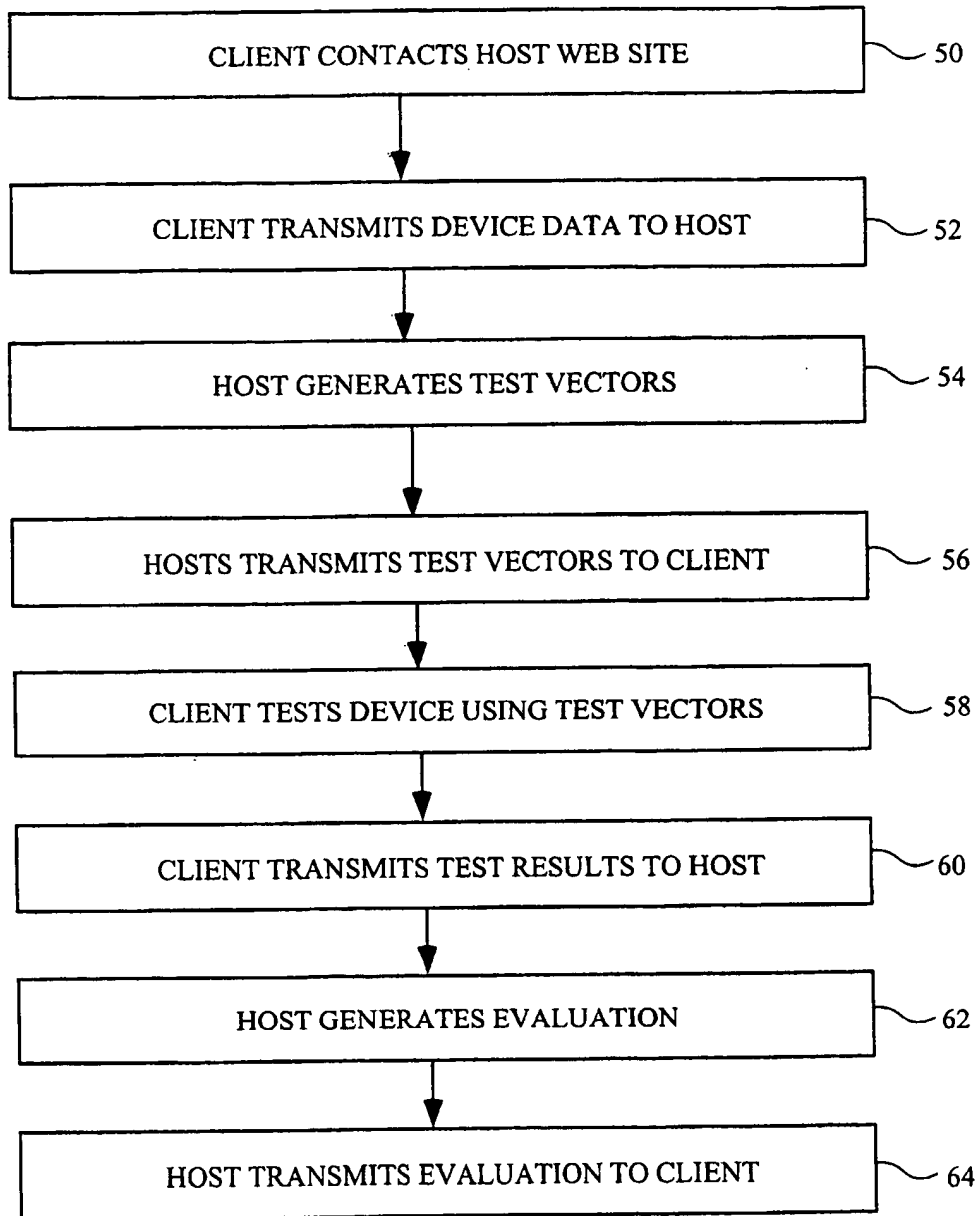


FIG. 2

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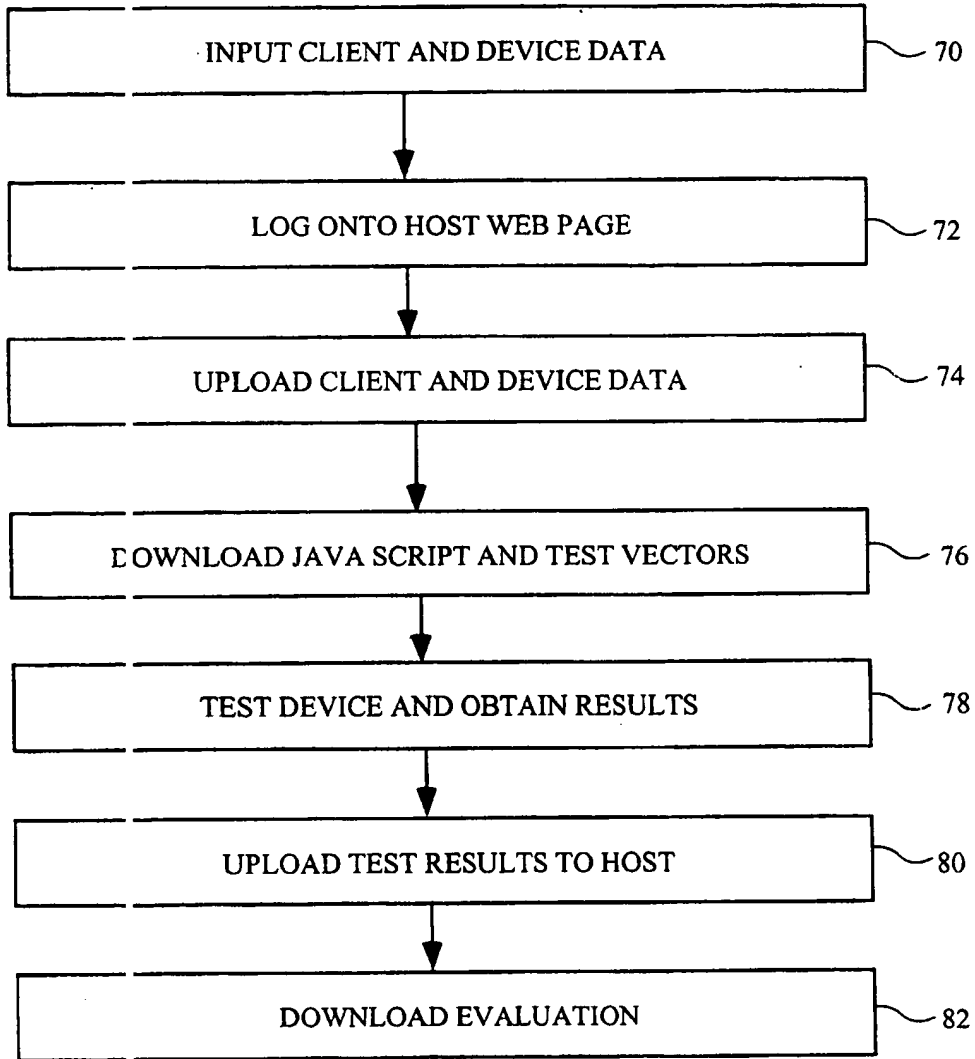


FIG. 3

4/4

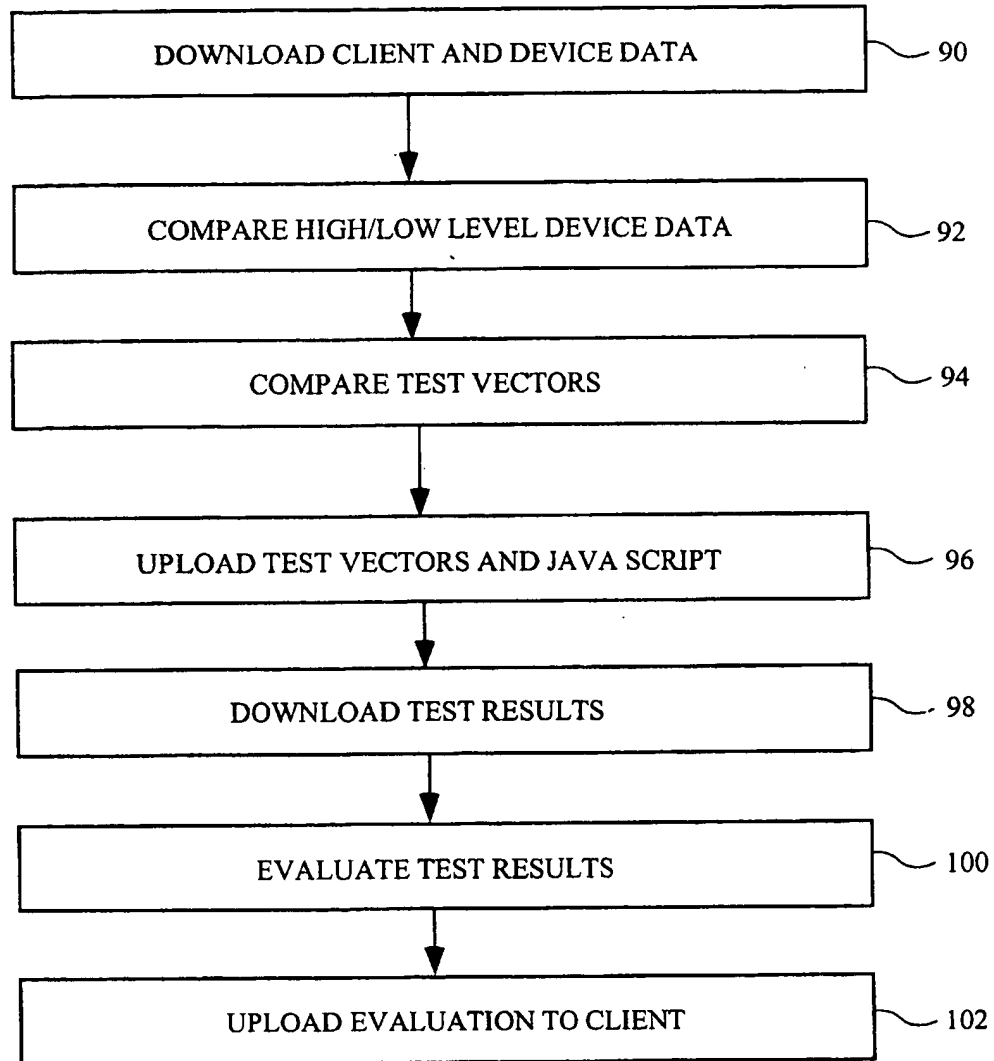


FIG. 4

INTERNATIONAL SEARCH REPORT

International Application No.

PCT/US 00/01326

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F 11/273

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 98 36356 A (ADVANCED MICRO DEVICES INC) 20 August 1998 (1998-08-20) abstract page 4, line 13 - line 26 page 6, line 1 - line 22 page 7, line 25 - line 28 page 9, line 4 - page 10, line 15	1-21
Y	US 5 630 048 A (DOBBS CARL S ET AL) 13 May 1997 (1997-05-13) column 3, line 65 - column 4, line 18 column 5, line 43 - line 47 column 12, line 23 - line 42 column 21, line 48 - line 62 column 23, line 53 - column 24, line 2	1-21
	-/-	

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

17 May 2000

Date of mailing of the international search report

31/05/2000

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INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>STAN RUNYON: "Silicon debug, scan tools go online" EETIMES, 'Online! 14 December 1998 (1998-12-14), XP002137881 Retrieved from the Internet: <URL:http://www.techweb.com/se/directlink.cgi?EET19981214S0042> 'retrieved on 2000-05-17! the whole document</p>	1-21

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